

**Amendments to and Listing of the Claims:**

Please cancel claims 13 and 20 and amend claims 2, 9-10, 15 and 17 as follows:

1. (Canceled)

2. (Currently amended)      A semiconductor device comprising:

an integrated circuit buffer having a delay generator, the buffer receiving ~~[[an]]~~ a clock input signal and generating a plurality of output signals that ~~relate to~~ are copies of the clock input signal delayed or advanced in time relative to the clock input signal, the delay generator being configured to phase-shift the timing of the plurality of output signals with respect to the clock input signal; and

a resistor having a resistance value, a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference, the resistor being external to the integrated circuit buffer, the resistance value determining a magnitude of the phase-shift caused by the delay generator.

3. (Original)    The device of claim 2 wherein the buffer comprises a zero-delay buffer.

4. (Original)    The device of claim 2 wherein the device is implemented on a circuit board and the external resistor is connected to a pin on a device package.

5. (Previously presented)      A semiconductor device comprising:

an integrated circuit buffer having a delay generator, the buffer receiving an input signal and generating a plurality of output signals that relate to the input signal;

a resistor having a first resistor end that is electrically connected to the delay generator and a second resistor end that is electrically connected to ground or a voltage reference, the resistor being external to the integrated circuit buffer; and

a plurality of internal capacitors which are used in conjunction with the external resistor to provide a timing reference, each capacitor having a first capacitor end that is electrically connected to a current source and a second capacitor end that is electrically connected to ground or a voltage reference.

6. (Previously presented) The device of claim 2 wherein:

the buffer further includes a phase locked loop, the phase locked loop including a phase detector; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of an internal feedback signal before the feedback signal reaches the phase detector.

7. (Original) The device of claim 6 wherein the plurality of output signals are phase-shifted to have a timing that is advanced relative to the input signal.

8. (Canceled)

9. (Currently amended) The device of claim 2, wherein:

the buffer further includes a phase locked loop, the phase locked loop including a phase detector; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of the clock input signal before the clock input signal reaches the phase detector.

10. (Currently amended) The device of claim 9 wherein the plurality of output signals are phase-shifted to have a timing that is retarded relative to the clock input signal.

11. (Canceled)

12. (Original) The device of claim 2 wherein:

the buffer includes a phase locked loop; and

the delay generator, a delay line and the external resistor are electrically connected to adjust the timing of one or more of the output signals exiting the phase locked loop to yield adjusted output signals.

13. (Canceled)

14. (Canceled)

15. (Currently amended) A method of adjusting the timing of an output signal of a semiconductor device, comprising:

electrically connecting a first terminal of an external resistor to a buffer that generates a plurality of output signals, the external resistor having a resistance value and the buffer including a delay generator and a phase locked loop, the first terminal of the external resistor being electrically coupled to the delay generator;

electrically connecting a second terminal of the external resistor to a ground or a voltage reference;

receiving a clock input signal in the buffer; ~~[[and]]~~

generating output signals from the buffer that are copies of the clock input signal delayed or advanced in time relative to the clock input signal; and

phase-shifting the timing of one or more of the output signals with respect to the clock input signal in an amount that is dependent upon the resistance value of the external resistor.

16. (Original) The method of claim 15 wherein the buffer comprises a zero-delay buffer.

17. (Currently amended) A semiconductor device comprising:

an input terminal that receives ~~[[an]]~~ a clock input signal;

a buffer that receives the input signal from the input terminal which is configured to generate a plurality of output signals that are copies of the clock input signal delayed or advanced in time relative to the clock input signal and to phase-shift the timing of at least one of the plurality of output signals with respect to the clock input signal; and

an external resistor coupled between the buffer and ground or a voltage reference, the external resistor having a resistance value that determines a magnitude of the phase-shift of at least one of the plurality of output signals relative to the clock input signal.

18. (Original) The device of claim 17 wherein the buffer comprises a zero-delay buffer.

19. (Original) The device of claim 18 wherein the device is implemented on a circuit board and the external resistor is connected to a pin on a package of the device.

20. (Canceled)

21. (Canceled)